Serial No.: 10/619,988

REMARKS

These remarks follow the order of the paragraphs of the office action. Relevant portions of the office action are shown indented and italicized. Claims 1-20 remain in the application. Claims are amended to better protect the invention. Some claims include insertions showing employment of Logical Communication Port architecture,

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 08/04/2005 have been fully considered but they are not persuasive.

2. Applicant mainly argues (i.e., on pg. 8 as well as pg. 10 of Remarks) that Garcia is only storing descriptors and not generating descriptors as specified by the claims.

Examiner does not agree. Garcia clearly provides mechanisms to generate/create plurality of the descriptors. Garcia discloses creating a linked list. e.g., a plurality of descriptors. Column 12, lines 62+ disclose creating/generating values in the descriptors in order to make up the link list. The chain pointer. Fig. 5 element 54, serves as a reference for locating and retrieving the next CDB as indicated in Column 13, lines 1-3. Column 14, lines 23+ disclose the multi-channel adapter unit generating the chain pointer in part to assist in establishing the linked list. Prior to these actions by Garcia, the descriptors were merely a random disparate collection of descriptors no necessarily associated with each other. In applicant's claims regarding the generation of descriptors, particularly claim 1, they recite simply "...descriptor logic for generating a plurality of descriptors including a frame descriptor defining a data packet to be communicated between a location in the memory and a second data processing system". Garcia covers this broad language. The descriptor logic is intrinsically present, represented by the hardware that performs the creation of values that go into each descriptor to form/generate the entire linked list, e.g., flow chart and hardware configurations shown in Figs. 6-11. The plurality of descriptors is indeed generated when the linked list is created which assembles and associate multiple descriptors together, by definition "generating a plurality of descriptors". Fig. 5, elements 52-54 shows the "frame

descriptor", since the elements 52-54 literally represent a frame where the information located within represent where the data block shown in Fig. 5, e.g., the data packet should go. Column 11, lines 1-25 disclose the MAU being a separate data processing system as Figure 1 shows the MAU clearly separated from other systems only to communicate with them over a bus, where the MAU processing the CDB which has the data pointer, element 52 that points the CDB to a location in the memory, element 3, indicated as the block storage space CDSB in Fig. 1. This is enough to meet "...frame descriptor defining a data packer to be communicated between a location in the memory and a second data processing system". The "pointer descriptor" as stated in the rejection can be identified as the data pointer in Fig. 5, element 52 since it points to the address/location in memory. Fig. 1, element 8. Lastly, the descriptor table is the CDT shown in Fig, 3, element 30, that is in the MAU, the second data processing system, that will be accessed by the memory and first processor, e.g., the first data processing system. The applicant argues the CDT as explicitly stated by Garcia is not a "descriptor table" but merely a table (pg. 10, last paragraph). Examiner points out that CDT stands for "channel descriptor table" and that the claim language only requires at least one of the descriptors to be in the CDT, not requiring everyone of the generated descriptors to be stored, even physically stored, in the table. Indeed, the head and tail pointers represent the linked list of CDBs in the CDT of Fig. 4 and thus meet the terminology of storing the descriptors in the table. Note also that the MAU puts the next CBD in the CDT based on what is the current CDB that is being processed (Fig. 7, element 73).

Nowhere in the claims disclose the details of what applicant construes as 'generating a plurality of descriptors', e.g. the applicant is apparently arguing the descriptors in their entirety are generated from scratch. However, under the broadest reasonable interpretation of the claims, this is not what the claim language state. The claims are sparse in defining what exactly "generating" descriptors entail. Garcia provides the act of adding/modifying the command descriptors and tables, and the fact that it assembles the plurality of descriptors into a linked list, all are enough to read on the applicants broad limitations regarding the generation of descriptors. Regarding the control of the flow of data between the memory of the host computer system and the data

communication interface, which the Examiner construes to be the MAU, the CDBs are transferred to the MAU as shown in Fig. 13, the CDB being fetched from memory. The fetches from the CDBs are based on the order of the linked list, and this is first initiated by the CDT having a pointer to the first CDB.

The applicants remaining arguments are along the same vein as what is answered above and also allege the use of hindsight. It is evident Garcia is anticipatory, showing all the elements of what is claimed in the instant application thus hindsight is not used. The Examiner reiterates his rejection in detail below.

In response, applicant respectfully takes exception with the statement above, "This is enough to meet "...frame descriptor defining a data packer to be communicated between a location in the memory and a second data processing system". The "pointer descriptor" as stated in the rejection can be identified as the data pointer in Fig. 5, element 52 since it points to the address/location in memory." These are apparently not the frame descriptor or pointer descriptor of the claims.

Claim Rejections- 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign county or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-20 rejected under 35 U.S.C. 102(b) as being anticipated by No. 5,448,702 Garcia.

In response, applicant respectfully states that a review of the cited portions of Garcia apparently fail to indicate that Garcia anticipates the invention claimed in claims 1-20.

5. As per claims 1 and 10, Garcia discloses an apparatus and method (Fig. 9) comprising: descriptor logic (Fig. 2-4 shown how descriptors are implemented, e.g. in

form a linked list and pointer; Fig. 5 shows the components of a descriptor), said apparatus for controlling flow of data between first and second data processing systems via a memory (Column 18, lines 53-65. The adapter in Fig. 9 is connected to the processor and memory which it assists in communications with DMA, the processor is in Fig. 1, element 2 and memory is Fig. 1, element 3, either the processor or the MAU adapter device can be construed to the first or second device), said descriptor logic for generating a plurality of descriptors including a frame descriptor defining a data packet to be communicated (Frame descriptor is shown in Fig. 5, element 52-55, where it dictates where to point the data to next and the amount of data in the packet) between a location in the memory and the second data processing system (Column 4, line 62-Column 5, line 10, where the apparatus in Fig. 5 transfers descriptors in memory to a plurality of peripheral devices, e.g., other data processing systems), and a pointer descriptor identifying the location in the memory (Fig. 5, element 52 or 54); and a descriptor table (Fig. 4) for storing the descriptors generated by the descriptor logic for access by the first and second data processing systems (contains a linked list of descriptors).

Applicants respectfully states that the present invention provides apparatus for controlling flow of data between first and second data processing systems via a memory, the apparatus comprising descriptor logic for generating a plurality of descriptors including a frame descriptor defining a data packet to be communicated between a location in the memory and the second data processing system, and a pointer descriptor identifying the location in the memory; and a descriptor table for storing the descriptors generated by the descriptor logic for access by the first and second data processing systems. The descriptor logic and descriptor table improve efficiency of data flow control between the first and second data processing systems such as a host computer system and a data communications interface for communicating data between the host computer system and a data communications network.

Garcia's invention is to provide a processor/adapter arrangement permitting a processor to dispatch CDB's serially from noncontiguous locations in a memory, for defining a series of data

transfer operation to be conducted in a continuously active adapter channel, wherein the dispatching functions of the processor can be discarded out without any coordination to activities in the respective channel and wherein the adapter invariably will perform the operations defined by the dispatched CDB's in a reliable manner, without compromising any activities in the respective channel. In accordance with Garcia, "a computer system and DMA (direct memory access) channel adapter are configured to cooperate in the formation and modification of linked list queues of chained descriptors/Con's while an adapter channel to which the respective queue is directed is active, and to carry out the queue formation/modification procedure in potentially optimal time coordination with the adapter's handling of data transfers relative to the respective channel and queue; whereby a COB can be added to or removed from a virtually empty queue (i.e. a queue whose CDB's have all been processed by the adapter) with minimal overall impact on processor and adapter performance."

Garcia apparently is only in regard to storing descriptors, not with generating descriptors **in entirety** as in claims 1 and 10. Thus the present invention and that of Garcia are clearly different, even though some same and/or similar words are used. Thus claims 1-20 are indeed allowable over Garcia.

A review of the cited portions of Garcia apparently fail to indicate that Garcia anticipates the invention claimed in claims 1-20. However, claims 1 and 10 are amended to specifically show that the plurality of descriptors are generated in entirety. The office action states that Garcia at the most, "provides the act of adding/modifying the command descriptors and tables including at least one newly generated descriptor." This is not the generating descriptors in claims 1 and 10.

Garcia is concerned with "permitting a processor to dispatch CDB's serially from noncontiguous locations in a memory, for defining a series of data transfer operation to be conducted in a continuously active adapter channel," not with flow control as in claim 1.

Garcia apparently does not refer to, and is not concerned with "generating in entirety a plurality of descriptors," nor with "a frame descriptor," nor with "defining a data packet to be

communicated between a location in the memory and the second data processing system," nor with, "a pointer descriptor identifying the location in the memory." The office action is apparently employing hindsight regarding the elements in Garcia's Figures 2-5, to construct the elements of claim 1. It is well established that hindsight may not be employed in rejecting a claim. Garcia apparently makes no reference to, nor is concerned with the invention of claim 1.

6. As per claims 2,3, 11 and 12, Garcia discloses claims 1 anti 10, wherein the descriptor table is stored in the data processing system (Fig. 3, stored in adapter registers. Fig. 9 is the MAU).

In response, applicant respectfully states that the office action is apparently unclear in regard to the rejection of claims 2, 3, 11 and 12 [and then claims 1 and 10]. It is noted that the remarks regarding apparatus claim 1, are similarly relevant for differentiating method claim 10 from Garcia. Thus claim 10, and all claims that depend on claim 10, are allowable over the cited art. Thus all claims are allowable over Garcia.

Apparently the elements of claims 1, 2, 3, 10, 11 and 12, are reconstructed by the office action into items in Garcia's Figs 3 and 9. The elements in claims 1, 2, 3, 10, 11 and 12 and the descriptor table for descriptors generated [claims 1 and 10] have little if any relationship to those in Garcia's figures. Thus, claims 1, 2, 3, 10, 11 and 12 are allowable over Garcia.

7. As per claims 4-6, 13 and 14, Garcia discloses claims 1 and 10, wherein the descriptor logic generates various branch descriptor comprising links to other descriptors in the descriptor table (Fig. 3, various descriptors shown branching/pointing to the next descriptor).

In response, applicant respectfully states that

Applicants respectfully state that it was shown above that Garcia indeed does not disclose claim 1 or claim 10. Garcia apparently does not generate any descriptors, nor refers to a cyclic descriptor list. The office action is apparently again employing hindsight regarding the elements

in Garcia's figures to construct the elements of claims 4-6, 13 and 14. It is well established that hindsight may not be employed in rejecting a claim. Thus Garcia indeed does not disclose the elements of claims 4-6, 13 and 14, which are all allowable in themselves and because each ultimately depends on an allowable claim.

8. As per claims 7 and 15, Garcia discloses claims 1 and 10, wherein the first data processing system comprises a host system (Fig. 1, processor 2 and memory 3 is the host processing system).

In response, applicants respectfully state that it was shown above that Garcia indeed does not disclose claim 1 or claim 10. There are indeed many patents that refer to a host system. Claims 7 and 15 are used for claim differentiation, and are indeed allowable in themselves and because each depends on an allowable claim.

9. As per claims 8 and 16, Garcia discloses claims 1 and 10, wherein the second data processing system comprises a data communications interface for communicating data between the host computer system and a data communication network (Column 9, lines 1-8, adaptors are attached external networks).

In response, applicants respectfully state that it was shown above that Garcia indeed does not disclose claim 1 or claim 10. A review of Garcia shows that Garcia is apparently not concerned with "a data communications interface for communicating data between the host computer system and a data communications network," of claims 8 and 16. These are not the adaptors of Garcia even if the adaptors may be attached external networks. Thus claims 8 and 16 are indeed allowable in themselves and because each depends on an allowable claim.

10. As per claim 9, Garcia discloses a data processing system (Fig. 1) comprising a host processing system having a memory (element 3), a data communications interface (Fig. 1, element 4.5) for communicating data between the host computer system and a data communication network (Column 9, lines 1-8), and apparatus according to claim 1.

In response, applicants respectfully state that the office action is apparently again employing hindsight regarding the elements in Garcia's figures to construct the elements of claim 9. It is well established that hindsight may not be employed in rejecting a claim.

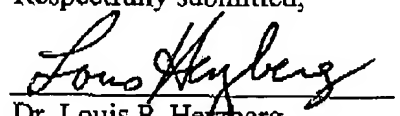
> *11. As per claims 17-20, Garcia discloses a computer program product, article of manufacture and program storage device readable by a machine (Fig. 1, shows computer product the result of manufacture, where the processor inherently requires initial instruction, e.g., booting and initialization, in order to start operation) in accordance to claims 1,9 and 10.*

In response, applicant respectfully take exception with the alleged showing in Garcia of a computer program product, article of manufacture and program storage device readable by a machine. Office action apparently is reading claims 17-20 into Garcia where these are apparently are not shown. Garcia shows no indication of the items in these Beauregard claims which protect the software etc.

It is anticipated that this amendment brings the application to allowance of claims 1-20, and favorable action is respectfully solicited. In the event that any claim remains rejected, please call the undersigned.

Please charge any fee necessary to enter this paper to deposit account 50-0510.

Respectfully submitted,

By: 

Dr. Louis P. Herzberg
Reg. No. 41,500
Voice Tel. (845) 352-3194
Fax. (914) 945-3281

3 Cloverdale Lane
Monsey, NY 10952

Customer Number: 54856